IN THE SPECIFICATION

Please replace the paragraph beginning at page 6, line 3 with the following paragraph:

The circuit 104 may be implemented as a controller circuit (e.g., a chip or integrated circuit) within the satellite set top box. The decoder 104 generally comprises a receiver block (or section) 120 and a processing block (or section) 122. The receiver block 120 may be implemented as a receiver chip connected to an antenna 124. The antenna 124 may be implemented as a satellite receiver antenna or other appropriate receiving device. For example, a typical residential environment uses a variety of satellite antennas such as 18 inch round dishes, 20 inch round dishes, 20 inch elliptical dishes, 22 inch elliptical dishes, etc. Additional satellite antennas are routinely developed (e.g., the multi-LNB "superdish" was recently announced). The present invention is not limited to a particular satellite antenna. The receiver 120 generally receives a signal from one of the low noise blockers (LNB) of the antenna 124. The receiver then presents a digital bitstream 130. In an alternate implementation, the digital bitstream 130 may be received from a cable television system.

Please replace the paragraph beginning at page 10, line 3 with the following paragraph:

The multiplexer 180 ~~164~~ may be digitally controlled. The signals ADJ1-ADJn may each have different effective capacitances. The multiplexer 180 ~~164~~ generally enables one of the signals ADJ1-ADJn to be selected to change the frequency of the signal CLK. The particular signal ADJ1-ADJn may be selected in response to the signal CTR. The signal CTR may be a software generated control signal. The embedded controller 160 may be implemented as a microprocessor or microsequencer.

Please replace the paragraph beginning at page 10, line 11 with the following paragraph:

Referring to FIG. 3, a more detailed diagram of the oscillator 162 and the tuning circuit 164 is shown. The tuning circuit 164 ~~162~~ is shown as a first portion 164a ~~162a~~ and a second portion 164b ~~162b~~. The oscillator 162 may be implemented as a DCXO (Digitally Controlled Crystal (Xtal) Oscillator). The oscillator 162 may pull up or down a main reference signal (e.g., REF). In one example, the main reference signal REF may be implemented as a 13.5MHz signal. However, other frequencies may be implemented to meet the design criteria of a particular implementation. The 13.5MHz reference signal REF may be used for the all of the Phase Locked Loops (PLLs) in a particular system. The tuning circuit 164a-164b may be used to adjust the signal REF. In one example, the tuning circuit 164a-164b ~~162a-162b~~ may make adjustments of

+150ppm and -150ppm. However, other adjustments may be used to meet the design criteria of a particular implementation.

Please replace the paragraph beginning at page 11,. line 5 with the following paragraph:

The oscillator 162 ~~160~~ is similar to a one inverter Pierce oscillator configuration. A gain stage generally acts as an active component to sustain the oscillations. For clarity, an inverter symbol 184 ~~180~~ is used in FIG. 3. A feedback resistor 186 ~~182~~, a number of capacitors C1-Cn and the crystal REF generally create a positive feedback, which starts the oscillation. The capacitors C1-Cn are placed symmetrically around the oscillator 162 ~~160~~. The capacitor banks C1-Cn are generally controlled digitally through a number of switches (e.g., D1-Dn). Depending on the code in the software 166, any of the switches D1-Dn may be turned on or off. Once a switch D1-Dn is turned on, the associated capacitor pair is connected to the both sides of the crystal REF. The oscillation frequency is inversely proportional to the capacitive load seen by the crystal REF. If the frequency of oscillation needs to be increased, one or more of the digital switches D1-Dn are turned off, until the desired frequency range is achieved. To decrease the frequency of oscillation, one or more of the switches D1-Dn have to be turned on. Since the switches D1-Dn can be

controlled easily from the software 166 through the controller 160 the turning off and on process may be software controllable.